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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JEFFREY S. MAILLOUX, KEVIN J. RYAN,
TODD A. MERRITT, and BRETT L. WILLIAMS

Appeal 2008-3076
Application 08/650,719
Technology Center 2100

Decided:[1] March 23, 2009

Before HOWARD BLANKENSHIP, JEAN R. HOMERE, and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

COURTENAY, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Data (electronic delivery).

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-9, 33-35, 46, 48-50, 59-61, 63, and 64. We have jurisdiction under 35 U.S.C. § 6(b). We AFFIRM IN PART.

INVENTION

The invention on appeal is directed generally to memory device architectures designed to provide high density data storage with high speed read and write access cycles. More particularly, Appellants' invention is directed to dynamic random access memory which is switch selectable between burst and pipelined modes. (Spec. 1).

ILLUSTRATIVE CLAIMS

Claims 1 and 61 illustrate the invention:

> 1. An asynchronously-accessible storage device comprising:
>
> mode circuitry configured to select between a burst mode and a pipelined mode; and
>
> circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.
>
> 61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:
>
> selecting a pipeline mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation;

switching modes to a burst mode of operation;

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation; and

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation.

PRIOR ART

The Examiner relies upon the following references as evidence in support of the obviousness rejections:

Ogawa	US 5,293,347	Mar. 8, 1994
Manning	US 5,610,864	Mar. 11, 1997
Roy	US 6,065,092	May 16, 2000

THE REJECTIONS

Claim 61 stands rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Manning and Roy.

Claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Manning and Ogawa.

We note that Appellants have not appealed the Examiner's double patenting rejection of claims 59-60, as set forth on pages 2-3 of the Final Office Action (*see* App. Br. 10).

GROUPING OF CLAIMS

(1) Appellants argue claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 as a group (App. Br. 13). We will, therefore, treat claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 as standing or falling with representative claim 1.

(2) Appellants argue claim 61 separately.

We accept Appellants' grouping of the claims. *See* 37 C.F.R. § 41.37(c)(1)(vii) ("Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any argument that the Board must consider the patentability of any grouped claim separately.").

RELATED APPEALS

Four prior BPAI Decisions on Appeal are noted with respect to this appeal:

1. *Ex parte Mailloux*, Appeal No. 2004-0414, decided on October 28, 2004.
2. *Ex parte Mailloux*, Appeal No. 2004-1705, decided on February 25, 2005.
3. *Ex parte Mailloux*, Appeal No. 2005-1725, decided on March 20, 2006.
4. *Ex parte Mailloux*, Appeal No. 2008-1916, decided on March 3, 2009.

Regarding the first three BPAI appeals, the same Manning reference relied upon in this present appeal was relied on with respect to rejections

under 35 U.S.C. § 102. "In reversing the rejections of substantially all claims in these three prior appeals, the various panels of the Board generally found that the lack of details with respect to Manning's teachings, at column 5, lines 43 through 46, relating to pipeline architectures of prior art memories, led to the conclusion that this reference alone did not suggest the specific applicability of the burst mode teachings of operation in Manning to these pipelined architectures." *Ex parte Mailloux*, No. 2008-1916, 2009 WL 537165 at *4 (BPAI 2009).

Appeal No. 2008-1916, decided on March 3, 2009, is closely related to this present appeal. We note that the identical Manning, Roy, and Ogawa references were relied on by the Examiner in Appeal No. 2008-1916, and essentially the same obviousness issues were considered by the previous BPAI panel.

35 U.S.C. § 112, 1st paragraph rejection of independent claim 61

Examiner's findings under 35 U.S.C. § 112, 1st paragraph

The Examiner finds that independent claim 61 recites subject matter which was not described in the Specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention, as follows:

1. The Examiner finds that the Specification does not disclose providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation (Ans. 6).
2. The Examiner finds that the Specification does not disclose switching modes to a burst mode of operation (*Id.*).

3. The Examiner finds that the Specification does not disclose while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation (*Id.*).
4. The Examiner finds that the Specification does not disclose providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation (*Id.*).

APPELLANTS' SPECIFICATION

Appellants point to the Specification at page 27, lines 1-11, page 38, lines 11-15, and page 39, lines 9-16, as providing support for the limitations found to be unsupported by the Examiner (App. Br. 11).

ISSUE

Have Appellants shown that the Examiner erred in rejecting claim 61 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement?

PRINCIPLES OF LAW

"Although [the applicant] does not have to describe exactly the subject matter claimed, the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed." *In re Gosteli*, 872 F.2d 1008, 1012 (Fed. Cir. 1989) (citations omitted). Put another way, "the applicant must . . . convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she

was in possession *of the invention*." *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991). Regarding the drawings as part of the Specification, "[t]he proper test is whether the drawings conveyed with reasonable clarity to those of ordinary skill that [the inventor] . . . invented . . . [the invention] . . . recited in those claims." *Id.* at 1566. The determination of whether a patent meets the written description requirement is a "question of fact, judged from the perspective of one of ordinary skill in the art as of the relevant filing date." *Falko-Gunter Falkner v. Inglis*, 448 F.3d 1357, 1363 (Fed. Cir. 2006) (citing *Vas-Cath,* 935 F.2d at 1563-64).

ANALYSIS

§ 112, first paragraph, written description

For convenience, we reproduce the portions of the Specification pointed to by Appellants here:

APPELLANTS' SPECIFICATION

> MUXs 124, 125. If newburst signal 110 is not active, memory 100 is in pipelined mode. As a result, XAO and XA1 are selected over signals 140, 141 as applied to MUXs 124, 125.
>
> In burst mode, newburst signal 110 is used to control counter 149 to load and increment values. Counter 149 loads address XAO and XAl. After a first /CAS signal 114 cycle in burst mode which uses the initial external values supplied for addresses XAO and XA1, counter 149 increments those initial values and provides new internally generated addresses A0 and A1 by supplying count 0 signal 140 and count 1 signal 141 to respective A0 and A1 locations in temporary storage 119 through MUXs 125, 124. In this manner, internal addresses may be generated based on an initial external address.

(Spec. 27, ll. 1-11).

> In column-based switching, switching between burst EDO and pipelined EDO modes is accomplished on successive /CAS cycles. Moreover, this type of switching may be accomplished on either read or write cycles, *e.g.,* from a burst EDO read cycle to a pipelined EDO read cycle and vise-versa, or from a burst EDO write cycle to a pipelined EDO write cycle and vise-versa.

(*Id.* at 38, ll. 11-15).

> In fixed access-based switching, burst address counter 149 (shown in FIG 9) may be employed for read operations, and external addressing may be employed for write operations. In other words, burst EDO mode may be used for read operations, and pipelined EDO mode may be used for write operations. In such a case, /WE signal 117 may be applied to mode circuitry 138 (shown in FIG. 11) such that when /WE signal 117 is logic low, memory 100 is in pipelined EDO mode, and when /WE signal 117 is logic high, memory 100 is in burst EDO mode. This implementation requires no redefinition of control signals.

(*Id.* at 39, ll. 9-16).

We consider the contested limitations in seriatim:

1. Providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation:

In addition to discussing the aforementioned portions of the Specification, Appellants aver that Figure 17 illustrates only some of the many possible embodiments and is not to be considered limiting all possible embodiments. (App. Br. 11).

After reviewing the aforementioned portions of the Specification proffered by Appellants as support, as well as Figure 17, we find sufficient disclosure that conveys with reasonable clarity to those skilled in the art possession of the aforementioned claimed subject matter. In particular, Figure 17 shows address data being provided during a pipelined mode of operation. Appellants' Specification further discloses that "[b]y pipelined EDO it is meant that an external address is used on each /CAS cycle for memory access . . . ." (Spec. 7, ll. 9-11).

Therefore, we find Appellants have shown the Examiner erred in determining that there is insufficient written description support for the limitations of *providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipeline mode of operation.*

2. Switching modes to a burst mode of operation:

After reviewing the aforementioned portions of the Specification proffered by Appellants as support, we find sufficient disclosure that conveys with reasonable clarity to those skilled in the art possession of the

argued limitations of *switching modes to a burst mode of operation*. In particular, we find Appellants' Specification discloses switching between burst EDO and pipelined EDO modes (Spec. 11). Appellants' Specification also discloses a newburst signal 110, that when active, memory 100 is in burst mode (*id.* at 26, l. 24). When newburst signal 110 is inactive, memory 100 is in pipelined mode (*id.* at 27, l. 1). Appellants further disclose that "either /OE signal 118, /WE signal 117, or P/B signal 120 may be used to provide newburst signal 110." (*Id.* at 27, l. 24 to 28, l. 1).

Therefore, we find Appellants have shown the Examiner erred in determining that there is insufficient written description support for the limitations of *switching modes to a burst mode of operation.*

3. While in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation:

As discussed *supra*, we have found Appellants have provided sufficient written description support for s*witching modes to a burst mode of operation* (i.e., from a pipelined mode and vice versa). Appellants' Specification also discloses generating internal addresses based on an initial external address when in burst mode (Spec. 27, l. 11). Therefore, we find Appellants have shown the Examiner erred in determining that there is insufficient written description support for the limitations of *while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.*

4. Providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation:

As discussed *supra*, Appellants' Specification discloses generating internal addresses based on an initial external address when in burst mode (Spec. 27, l. 11). Thus, only one external address is provided for each burst access. Therefore, we find Appellants have shown the Examiner erred in determining that there is insufficient written description support for the limitations of *providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the burst mode of operation.*

CONCLUSION (*35 U.S.C. §112, first paragraph rejection*)

For at least the aforementioned reasons, we find Appellants have shown the Examiner erred. Therefore, we reverse the Examiner's rejection of claim 61 under 35 U.S.C. § 112, first paragraph.

35 U.S.C. § 103(a) rejections

Claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64

APPELLANTS' CONTENTIONS

Appellants contend that there is "nothing in Manning to suggest substituting a pipelined mode for the page mode, as suggested by the Office with respect to Ogawa" (App. Br. 15, para. 4). Appellants further contend that "no combination of Manning and either Roy or Ogawa can provide 'choosing whether the memory is in a burst mode of operation or a pipelined mode of operation' or 'selecting a burst or a pipeline mode of operation,'

much less 'mode circuitry configured to select between a burst mode and a pipelined mode,' as claimed . . . ." (*Id.* at 15-16).

In addition, Appellants argue that the Manning and Roy references and the Manning and Ogawa references have not been properly combined by the Examiner (*id.* at 16-17).

EXAMINER'S RESPONSE

In the "Response to Arguments" section of the Answer, the Examiner maintains that the limitations argued by Appellants are taught and/or suggested by the first proffered combination of Manning and Roy and the second proffered combination of Manning and Ogawa (Ans. 30-34).

In particular, the Examiner acknowledges that the primary Manning reference does not specifically discuss the detailed operation of a pipeline mode. However, the Examiner maintains that it is well known in the memory art that the pipelined memory architecture provides several advantages, e.g., speed, overlapped operations, cost savings, etc. (*Id.* at 31-32).

In addition, the Examiner maintains that the Manning and Roy and Manning and Ogawa references have been properly combined (*Id.* at 34-37).

ISSUES

We consider the following issues that flow from the contentions of the Appellants and the Examiner:

1. Have Appellants shown that the Examiner erred in finding that the Manning and Roy references and also the Manning and Ogawa references are combinable under 35 U.S.C. § 103?

2. Have Appellants shown that the Examiner erred in finding that the combination of Manning and Roy and, separately, the combination of Manning and Ogawa, teaches the argued feature of mode circuitry configured to select between a burst mode of operation and a pipelined mode of operation in a memory?

PRINCIPLES OF LAW

"What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid under § 103." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). To be nonobvious, an improvement must be "more than the predictable use of prior art elements according to their established functions." *Id.* at 1740.

FINDINGS OF FACT

In our analysis *infra*, we rely on the following findings of fact (FF) that are supported by a preponderance of the evidence:

THE PRIMARY MANNING REFERENCE

1. Manning teaches the ability to switch between burst EDO and standard EDO modes of operation of memory devices. (Col. 6, ll. 14-16).

2. Manning teaches "[o]ther memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete." (Col. 5, ll. 41-45).

3. Manning teaches "[i]n the burst access memory device, each new column address from the column address counter is decoded and is used to access additional data within the memory array without the requirement of additional column addresses being specified on the address inputs 16." (Col. 5, ll. 51-54) (bolding omitted).

4. Manning teaches "[o]ther possible alterations in the feature sets of this DRAM include having a fixed burst mode only, selecting between standard fast page mode (non-EDO) and burst mode, and using the output enable pin (/OE) 42 in combination with /RAS to select between modes of operation." (Col. 7, ll. 43-47) (bolding omitted).

5. Manning teaches "[a] more complex memory device may provide additional modes of operation such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time." (Col. 7, ll. 49-53).

6. Manning teaches "[a]lternately, a device with multiple modes of operation may have wire bond locations, or programmable fuses

which may be used to program the mode of operation of the device." (Col. 7, ll. 56-59).

THE SECONDARY ROY REFERENCE

7. Roy teaches that "[t]he architecture of the present application can support various types of transactions, including a row burst access, a column burst access, a background row change, a pipelined random column access, and refresh operations." (Col. 27, ll. 54-57).

8. Roy teaches that "[f]or a given type of transaction, the particular operating mode of the selected channel and cluster of the memory device 20 is defined by the protocol by which information packets are configured. According to the protocol, each transaction is initiated by a header that includes certain address and control information regarding the routing of data." (Col. 28, ll. 36-39) (bolding omitted).

9. Roy teaches that "[r]eferring now to FIGS. 8 through 12, exemplary header formats for various types of read and write transactions are illustrated, including a row burst access (FIG. 8), a background row change (FIG. 9), a column burst access (FIG. 10), a pipelined random column mode (FIG. 11), and a pair of pipelined random column write address/data packets (FIG. 12)." (Col. 28, ll. 48-54) (bolding omitted).

THE SECONDARY OGAWA REFERENCE

10. Ogawa teaches a "dynamic type semiconductor memory device [for] carrying out pipe line processing in page mode . . . ." (Abstract).

11. Ogawa teaches that "pipe line processing is particularly effective in a dynamic type semiconductor memory device carrying out page mode processing to realize high speed operation." (Col. 3, ll. 52-54).

12. Ogawa teaches that "[i]f pipe line processing can be carried out under page mode in a dynamic type semiconductor memory device, high speed operation in reading and the like can be expected." (Col. 4, ll. 9-12).

ANALYSIS

35 U.S.C. § 103 rejections

ISSUE 1

Combinability of the cited references

We decide the question of whether Appellants have shown that the Examiner erred in finding that the Manning and Roy references and also the Manning and Ogawa references are combinable under 35 U.S.C. § 103.

Appellants have asserted that (1) there is no motivation to combine the cited references, that (2) Manning teaches away from the asserted combination, and (3) that there would have been no reasonable expectation of success in combining the references in the manner proffered by the Examiner. (App. Br. 16-17).

We have fully considered Appellants' arguments as presented in the Briefs. However, after reviewing the evidence before us, we find several

factors that support the Examiner's conclusion of obviousness. When analyzing the present case, we consider a variety of reasons that may have led one skilled in the art to combine the teachings of Manning and Roy (and Manning and Ogawa) in the manner proffered by the Examiner. We preface our analysis by noting that the Supreme Court has clearly stated that "any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *KSR*, 127 S. Ct. at 1742.

At the outset, we note that Manning, Roy, and Ogawa are each directed to improved Dynamic Random Access Memory (DRAM) architectures. Therefore, we find Manning, Roy, and Ogawa are each analogous art directed to the same field of endeavor as Appellants' invention.[2]

Moreover, contrary to Appellants' arguments, we find the Examiner has not looked to the secondary Roy and Ogawa references for the purpose of bodily incorporating their specific structural details into the particular memory structure of Manning. Instead, we find the Examiner has merely looked to the Roy and Ogawa references for their general teaching of

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[2] "Whether a reference in the prior art is 'analogous' is a fact question." *In re Clay*, 966 F.2d 656, 658 (Fed. Cir. 1992) (citing *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1568 n.9 (Fed. Cir. 1987)). Two criteria have evolved for answering the question: "(1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved." *Id.* at 658-59 (citing *In re Deminski*, 796 F.2d 436, 442 (Fed. Cir. 1986)).

pipelined modes and the advantages of pipelined modes that the Examiner considers to be well known in the art, e.g., speed, overlapped operations, cost savings, etc. (*See* Ans. 31-32).

Thus, it is our view that Appellants' arguments do not take into account what the collective teachings of the prior art would have suggested to one of ordinary skill in the art and are therefore ineffective to rebut the Examiner's prima facie case of obviousness. "What appellants overlook is that it is not necessary that the inventions of the references be physically combinable to render obvious the invention under review." *In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. United States*, 702 F.2d 1005, 1013 (Fed. Cir. 1983)); *See In re Keller*, 642 F.2d 413, 425 (CCPA 1981) ("*The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference*; *nor is it that the claimed invention must be expressly suggested in any one or all of the references.* Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.") (emphasis added). *See also In re Nievelt*, 482 F.2d 965, 968 (CCPA 1973) ("Combining the *teachings* of references does not involve an ability to combine their specific structures."). This reasoning is applicable in the present case.

The Supreme Court has further stated that "[c]ommon sense teaches . . . that familiar items may have obvious uses beyond their primary purposes, and . . . a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *KSR*, 127 S. Ct. at 1742. Courts should "take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.* at 1741.

Here, it is our view that an artisan at the time of the invention would have been familiar with dynamic random access memories that were capable of operating in burst or pipelined modes. Therefore, we find that it would have been common sense for an artisan familiar with Manning's ability to switch between burst and standard EDO modes (FF 1) to have looked to the secondary Roy and Ogawa references for their general teachings of DRAM pipelined modes of operation, given that Manning expressly teaches that "[o]ther memory architectures applicable to the current invention include a pipelined architecture where memory accesses are performed sequentially, but each access requires more than a single cycle to complete." (FF 2).

Moreover, we note that Appellants have not rebutted the Examiner's legal conclusion of obviousness by showing that the claimed combination of familiar elements produces any new function. Appellants have not provided any factual evidence of secondary considerations, such as unexpected or unpredictable results, commercial success, or long felt but unmet need.

For at least the aforementioned reasons, we find Appellants' arguments unpersuasive that the cited references have been improperly combined by the Examiner.

ISSUE 2

Claimed Limitations

We decide the question of whether Appellants have shown that the Examiner erred in finding that the combination of Manning and Roy and, separately, the combination of Manning and Ogawa, teaches the argued feature of mode circuitry configured to select between a burst mode of operation and a pipelined mode of operation in a memory.

At the outset, based upon our review of the references, we agree with Appellants that the Manning, Roy, and Ogawa references do not expressly teach switching between a burst mode and a pipelined mode (*see* App. Br. 14). We acknowledge that the primary Manning reference merely teaches the ability to switch between burst EDO and standard EDO modes of operation (FF 1), and other non-pipelined modes (FF 4).

Nevertheless, we find that Manning clearly teaches the general concept of mode switching in the dynamic random access memory art (FF 1, 4, 5). We also find that Manning clearly indicates the applicability of pipeline architectures to his invention (*see* FF 2), thus providing a compelling suggestion to the reasonably skilled artisan that both burst and pipelined modes could be implemented.

Therefore, we see the question before us to be whether a reasonably skilled artisan, having knowledge of the teachings of Manning, Roy, and Ogawa, would have found it obvious to fill the gap in the teachings of Manning by modifying the EDO mode switching to switch between burst and pipelined modes of operation.

The Supreme Court has found that "[i]n making the determination of 'obviousness,' it is important to remember that the criterion is measured not in terms of what would be obvious to a layman, but rather what would be obvious to one 'reasonably skilled in (the applicable) art.'" *Dann v. Johnston*, 425 U.S. 219, 229 (1976) (quoting *Graham v. John Deere Co.*, 383 U.S. 1, 37 (1966)). In *Dann*, the Supreme Court reached a finding of obviousness by concluding that "[a]ssuming such an awareness, respondent's system would . . . have been obvious to one 'reasonably skilled in (the applicable) art'" even though, as the court explicitly noted, "[t]here

may be differences between respondent's invention and the state of the prior art." *Id.* at 229 (quoting *Graham*, 383 U.S. at 37). In particular, we note that the Supreme Court held in *Dann* that "the mere existence of differences between the prior art and an invention does not establish the invention's nonobviousness . . . [where] [t]he gap between the prior art and respondent's system is simply not so great as to render the system nonobvious to one reasonably skilled in the art." *Id.* at 230 (holding that claims directed to a machine system for automatic record keeping of bank checks and deposits were obvious in view of the use of data processing equipment and computer programs in the banking industry at the time of the invention in combination with a prior art automatic data processing system using a programmed digital computer for use in a large business organization).

Here, we agree with the Examiner that the respective advantages of pipeline (and burst) modes of DRAM operation were known to the artisan and are established by the teachings of the cited references. We find Manning provides abundant suggestions to the artisan by teaching that "a more complex memory device may provide additional modes of operation" (FF 5), and also that a memory device may have multiple modes of operation (FF 6), where a selection may be made between various modes (FF 4). We find the secondary Roy and Ogawa references clearly evidence various aspects of pipelined DRAM operation that would have been known to an artisan at the time of the invention (FF 7-12).

After considering the totality of the evidence before us, it is our reasoned view that the gap between the prior art and Appellants' claimed invention is simply not so great as to render Appellants' system nonobvious to one reasonably skilled in the dynamic random access memory art.

Moreover, we find it reasonable that an artisan, having knowledge of the teachings of Manning, Roy, and Ogawa, would have found it obvious to try modifying Manning's mode circuitry to switch between a burst mode of operation and a pipelined mode of operation (as taught by Roy and Ogawa) to reach Appellants' claimed invention.

Under *KSR*, it is now apparent that "obvious to try" may be an appropriate test in more situations than we previously contemplated: [3]

> When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under § 103.

KSR, 127 S. Ct. at 1742.

This reasoning is applicable here. After considering the totality of the evidence before us, it is our reasoned view that an artisan having common sense and creativity would have pursued the known options (i.e., a burst mode switched to a pipelined mode) within his or her technical grasp. Based on the evidence before us, we find no more ingenuity and skill would have been required to make such an improvement than would have been possessed by a reasonably skilled artisan acquainted with the dynamic random access memory art.

"Invention or discovery is the requirement which constitutes the foundation of the right to obtain a patent . . . unless more ingenuity and skill

[3] *See Ex parte Kubin*, 83 USPQ2d 1410, 1414 (BPAI 2007) (Precedential).

were required in making or applying the said improvement than are possessed by an ordinary mechanic acquainted with the business, there is an absence of that degree of skill and ingenuity which constitute the essential elements of every invention." *Dunbar v. Myers*, 94 U.S. 187, 197 (1876) (citing *Hotchkiss* v. *Greenwood*, 52 U.S. 248, 267 (1850)) (*Hotchkiss* v. *Greenwood* was cited with approval by the Supreme Court in *KSR*, 127 S. Ct. at 1734, 1739, 1746).

For at least the aforementioned reasons, we find Appellants have not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of representative claim 1 as being unpatentable over either Manning in view of Roy or Manning in view of Ogawa. Claims 2-9, 33-35, 46, 48-50, 59-60, 63, and 64 fall therewith.

CONCLUSION

Based on the findings of facts and analysis above, Appellants have established that the Examiner erred in rejecting claim 61 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Based on the findings of facts and analysis above, Appellants have not established that the Examiner erred in rejecting claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 as being unpatentable over the combination of Manning and Roy under 35 U.S.C. § 103(a).

Based on the findings of facts and analysis above, Appellants have not established that the Examiner erred in rejecting claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64 as being unpatentable over the combination of Manning and Ogawa under 35 U.S.C. § 103(a).

DECISION

We reverse the Examiner's rejection of claim 61.

We affirm the Examiner's rejection of claims 1-9, 33-35, 46, 48-50, 59-60, 63, and 64.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

msc

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